

深圳市阿美林电子科技有限公司

Specification

TFT-LCD module

Module(型号):	AML-FRD15424IPS
Customer（客户）：	
Customer P/N（客户型号）：	

If there is no special request from customer, will not reserve the tooling of the product under the following conditions:  
1.There is no response from customer in one years after SHENZHEN AMELIN Electronics Technology CO.,LTD submit The samples;  
2.There is no order in one years after the latest mass production.And correlated data (include quality record) will be reserved one year more after tooling was discarded.

Approved by（批准）：	
Qualified（合格）：	Unqualified（不合格）：

PREPARED	CHECKED	APPROVED

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## REVISION RECORD

<u>REV NO</u>	<u>REV DATE</u>	<u>CONTENTS</u>	<u>REMARKS</u>
1.0	2014-12-9	First Release	
2.0	2015-1-12	Second Release	

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## 1.0 General Specifications

**AML-FRD15424IPS** is a color active matrix LCD module incorporating amorphous silicon **TFT** (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, FPC and a back light unit. The module display area contains **240x 240** pixels and can display up to **262K** colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit
LCD Type	TFT TRANSMISSIVE	/
Viewing direction	ALL DIRECTION	O' Clock
Module outline (W x HxD)	31.52*33.72*1.32	mm
Active area (WxH)	27.72*27.72	mm
Number of Dots	240(RGB) x240	/
Driver IC	ST7789H	/
Colors	262K	/
Backlight Type	LED	/
Interface Type	MCU 8 BIT	/
Input voltage	2.8	V
Appearance standard	No spot and No scratching in Active area	/

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## 2.0 ABSOLUTE MAXIMUM RATINGS

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
Supply voltage for logic	Vcc1,Vcc2	-0.3	4.6	V
Input voltage	Vin	0.5	VCC+ 0.5	V
Operating temperatur	Top	-20	60	°C
Storage temperature	Tst	-30	70	°C
Humidity	RH	--	90%(Max60C)	RH

## 3.0 ELECTRICAL CHARACTERISTICS

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Supply voltage for logic	Vcc -Vss	2.4	2.8	3.2	V
I/O power supply	IOVCC	1.65	1.8	3.2	V
Input Current	Idd	-	TBD	TBD	mA
Input voltage 'H' level	Vih	0.7IOVCC	--	IOVCC	V
Input voltage 'L' level	Vil	GND	0	0.3IOVCC	V
Output voltage 'H' level	Voh	0.8IOVCC	--	IOVCC	V
Output voltage 'L' level	Vol	GND	0	0.2IOVCC	V

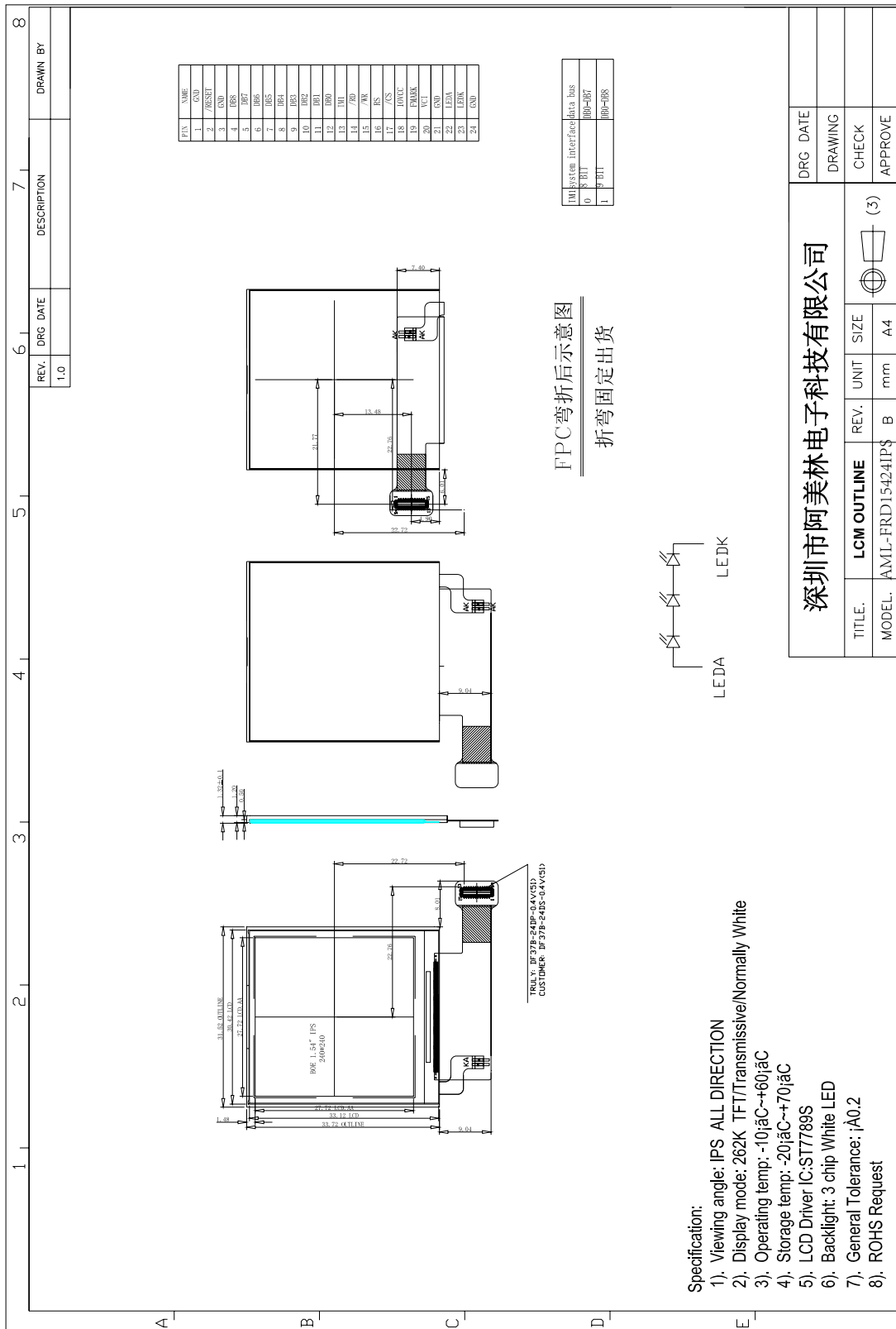
## 4.0 BACKLIGHT CHARACTERISTICS

<i>Item</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Condition</i>
Forward voltage	Vf	7.8	9.0	10.0	V	--
Luminance	Lv	3500	3800	4200	cd/m2	If=15mA
Number of LED	--	3			Piece	--
Connection mode	S	Serial			--	--

Using condition: constant current driving method If= 15mA(+/-10%)

## 5.0 DIMENSIONAL DRAWING

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## 6.0 INTERFACE PIN CONNECTIONS

<i><b>Pin.No</b></i>	<i><b>Symbol</b></i>	<i><b>Function</b></i>
1	GND	Ground
2	RESET	A reset pin
3	GND	Ground
4	DB8	Data bit
5	DB7	Data bit
6	DB6	Data bit
7	DB5	Data bit
8	DB4	Data bit
9	DB3	Data bit
10	DB2	Data bit
11	DB1	Data bit
12	DB0	Data bit
13	IM1	8/9BIT system select pin
14	RD	Read data input pin
15	WR	Write data input pin
16	RS	data or command select signal input
17	CS	chip select signal input
18	IOVCC	power supply (1.8/+2.8)
19	FMARK	Tearing effect signal is used to synchronize MCU to frame memory writing
20	VCI	Power supply (+2.8)
21	GND	Ground
22	LEDA	Back light power supply positive
23	LEDK	back light power supply negative
24	GND	Ground

## 6.1 TIMING CHARACTERISTICS

### 6.1.1 Serial interface characteristics (4-line serial)

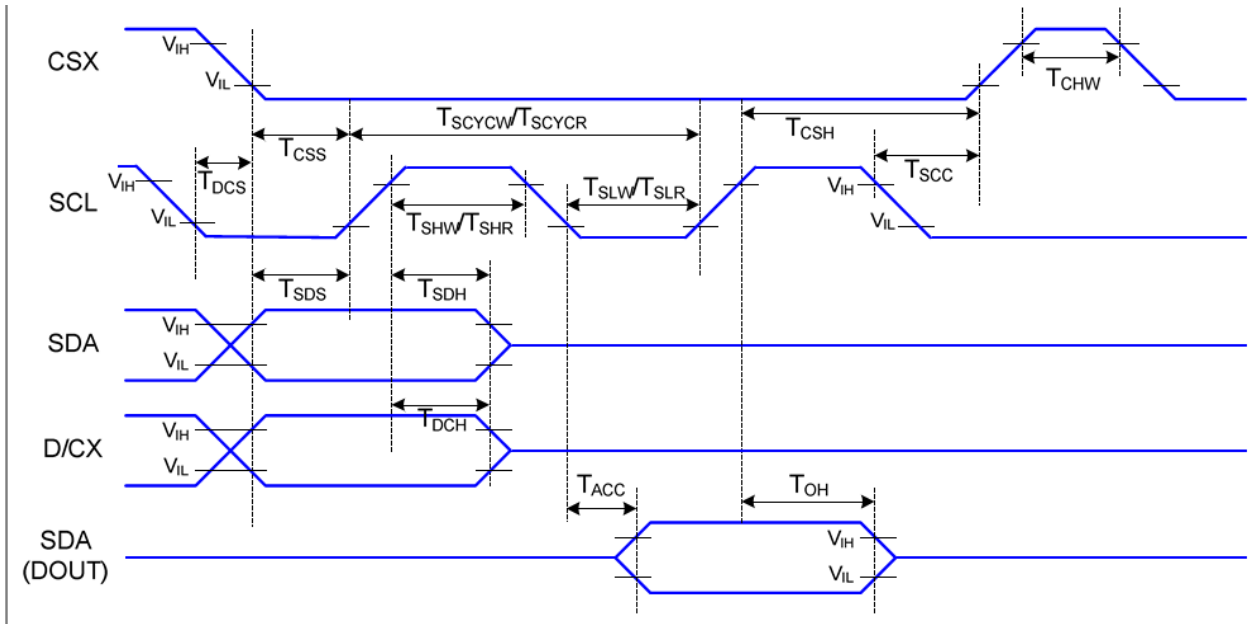


Figure 8.4.1 4-line serial interface timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time (write)	45		ns	
	T <sub>CSH</sub>	Chip select hold time (write)	45		ns	
	T <sub>CSS</sub>	Chip select setup time (read)	60		ns	
	T <sub>SCC</sub>	Chip select hold time (read)	65		ns	
	T <sub>CHW</sub>	Chip select "H" pulse width	40		ns	
SCL	T <sub>SCYCW</sub>	Serial clock cycle (Write)	66		ns	-write command & data ram
	T <sub>SHW</sub>	SCL "H" pulse width (Write)	15		ns	
	T <sub>SLW</sub>	SCL "L" pulse width (Write)	15		ns	
	T <sub>SCYCR</sub>	Serial clock cycle (Read)	150		ns	-read command & data ram
	T <sub>SHR</sub>	SCL "H" pulse width (Read)	60		ns	
	T <sub>SLR</sub>	SCL "L" pulse width (Read)	60		ns	
D/CX	T <sub>DCS</sub>	D/CX setup time	10		ns	
	T <sub>DCH</sub>	D/CX hold time	10		ns	
SDA (DIN) (DOUT)	T <sub>SDS</sub>	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	T <sub>SDH</sub>	Data hold time	10		ns	
	T <sub>ACC</sub>	Access time	10	50	ns	
	T <sub>OH</sub>	Output disable time	15	50	ns	

Table 8.4.1 4-line Serial Interface Characteristics



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## 6.2. Reset Input Timing

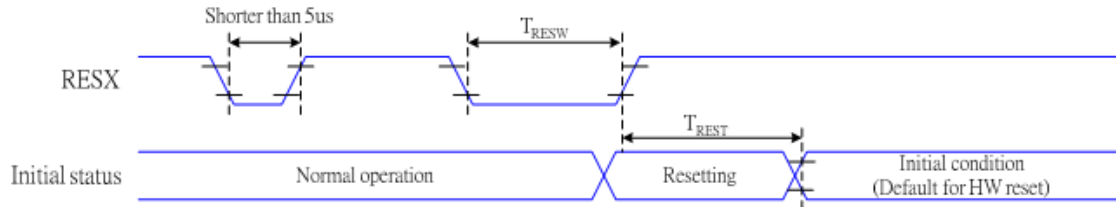


Table 9.16.1 Reset timing

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	$\overline{RESW}$	Reset pulse duration	10	-	us
	$\overline{tREST}$	Reset cancel	-	5	ms
				120	ms

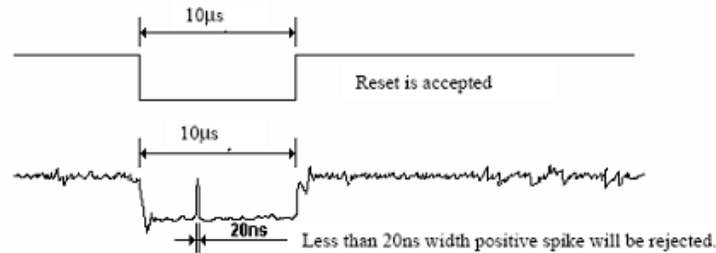
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

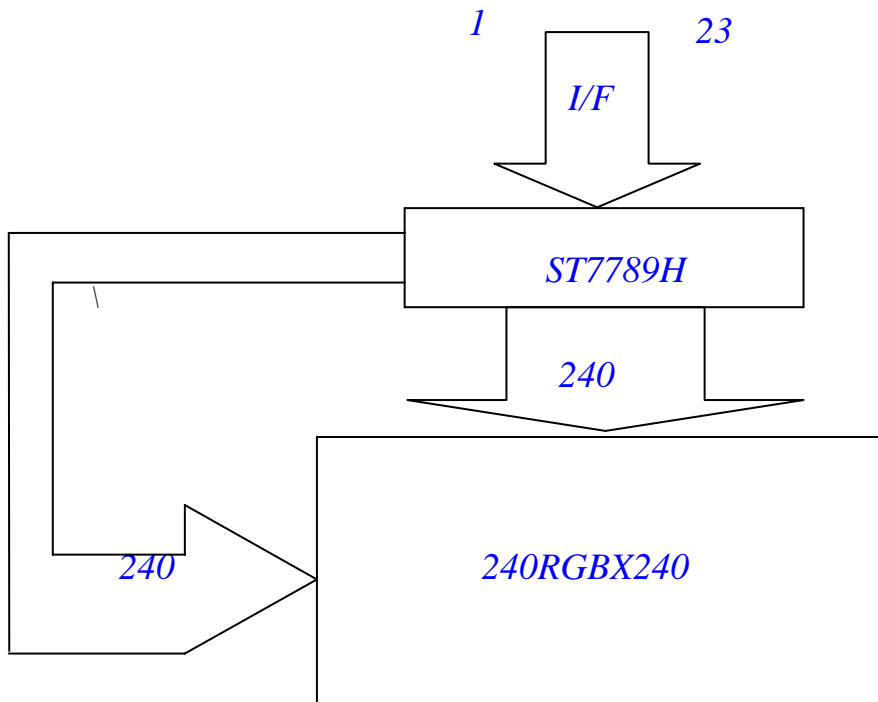
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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## 6.3 BLOCK DIAGRAM OF LCM



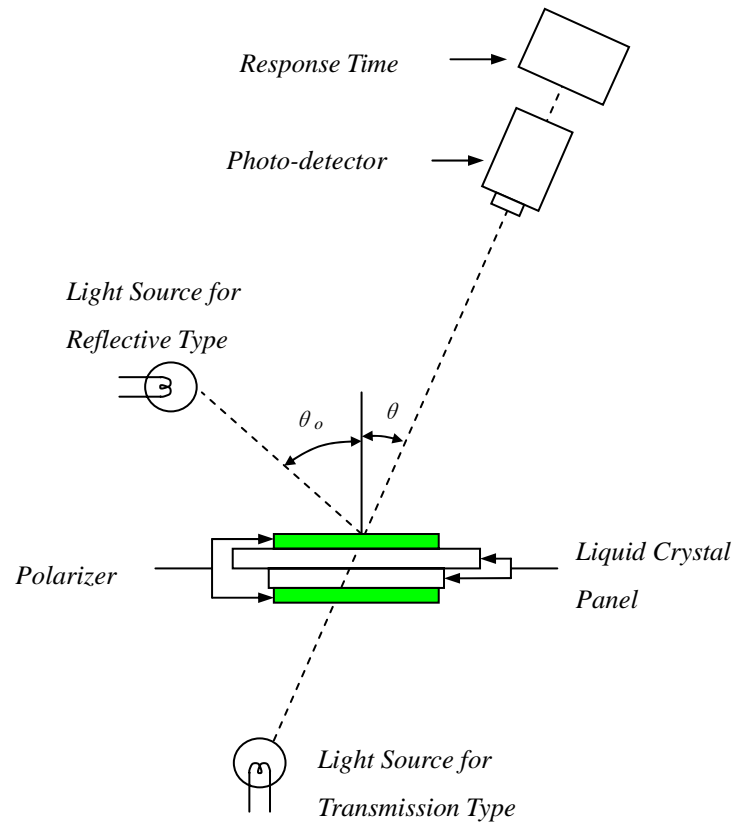
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## 7. *ELECTRO-OPTICAL CHARACTERISTICS*

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold Voltage		Vsat		4.1	4.3	4.5	V	Fig.1
		Vth		1.6	1.8	2.0	V	
Viewing Angle	Horizontal	Θ3	CR>10		80		°	Note 1
		Θ9			80		°	
	Vertical	Θ12			80		°	
		Θ6			80		°	
Contrast Ratio		CR	Θ= 0°		900			Note 2
Transmittance		T(%)	Θ= 0°		6.4			Note 3
NTSC		%	Θ= 0°		50			
Reproduction Of color	Red	Rx	Θ= 0°		TBD			Note 4 *CF glass
		Ry			TBD			
	Green	Gx			TBD			
		Gy			TBD			
	Blue	Bx			TBD			
		By			TBD			
White		Wx	Θ= 0°		TBD			
		Wy			TBD			
Response Time		Tr+Tf	Θ= 0°		35	50	ms	Note 5

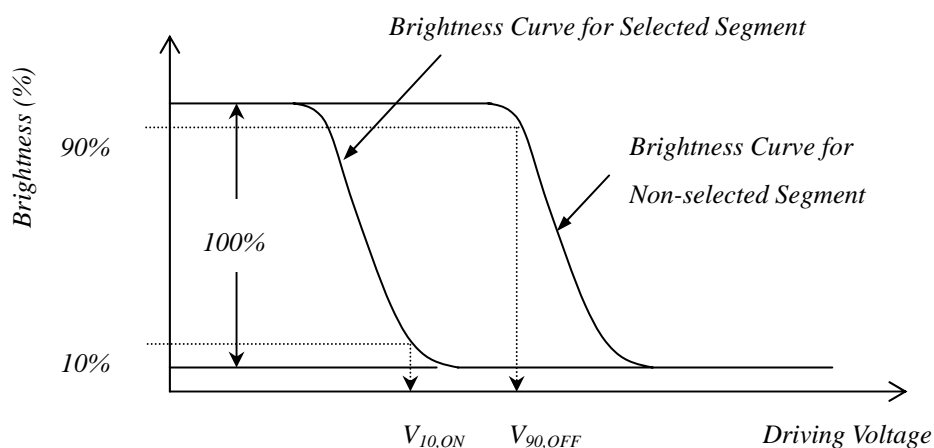
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## 7.1 ELECTRO-OPTICAL CHARACTERISTICS TEST METHOD

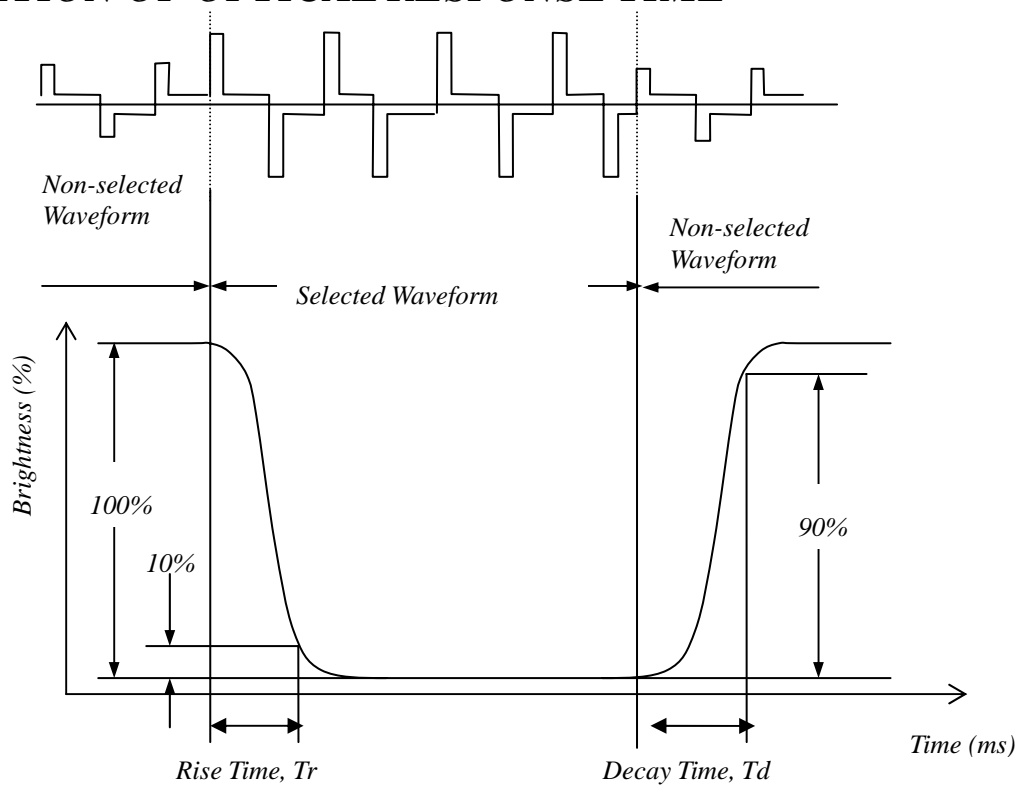


## 7.2 DEFINITION OF OPERATING VOLTAGE, VOP

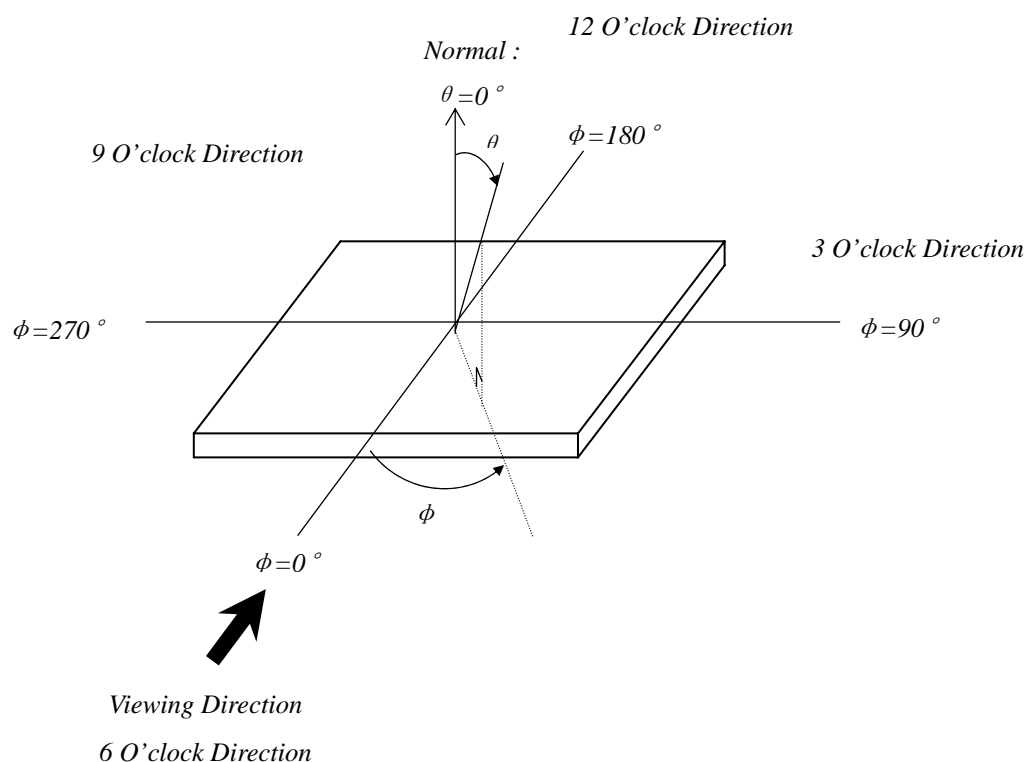
$$V_{op} = (V_{10,ON} + V_{90,OFF})/2$$



## 7.3 DEFINITION OF OPTICAL RESPONSE TIME

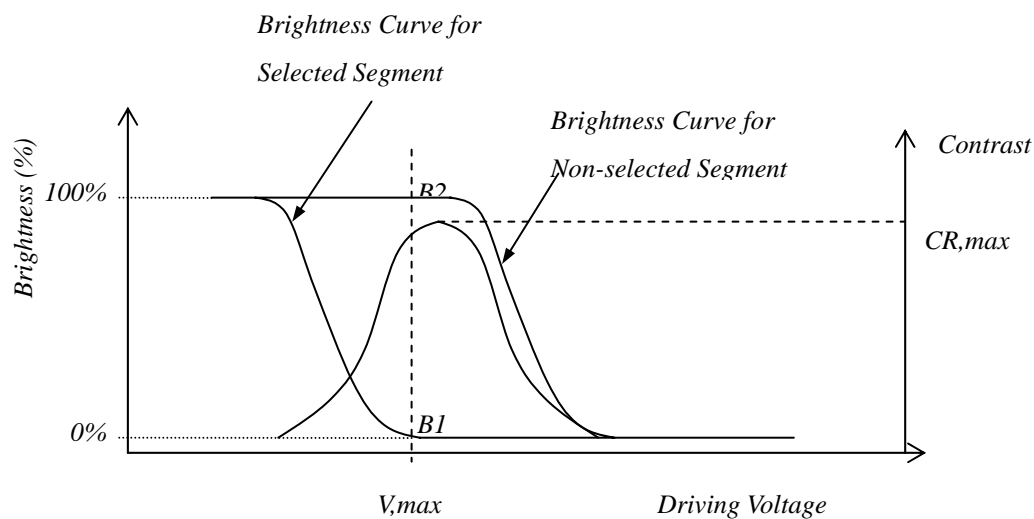


## 7.4 DEFINITION OF VIEWING ANGLE $\theta$ AND



## 7.5 DEFINITION OF CONTRAST RATIO, CR

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$



## 8.INSPECTION CRITERIA

### 8.1 Inspection Conditions

#### 8.1.1 Environmental conditions

*The environmental conditions for inspection shall be as follows*

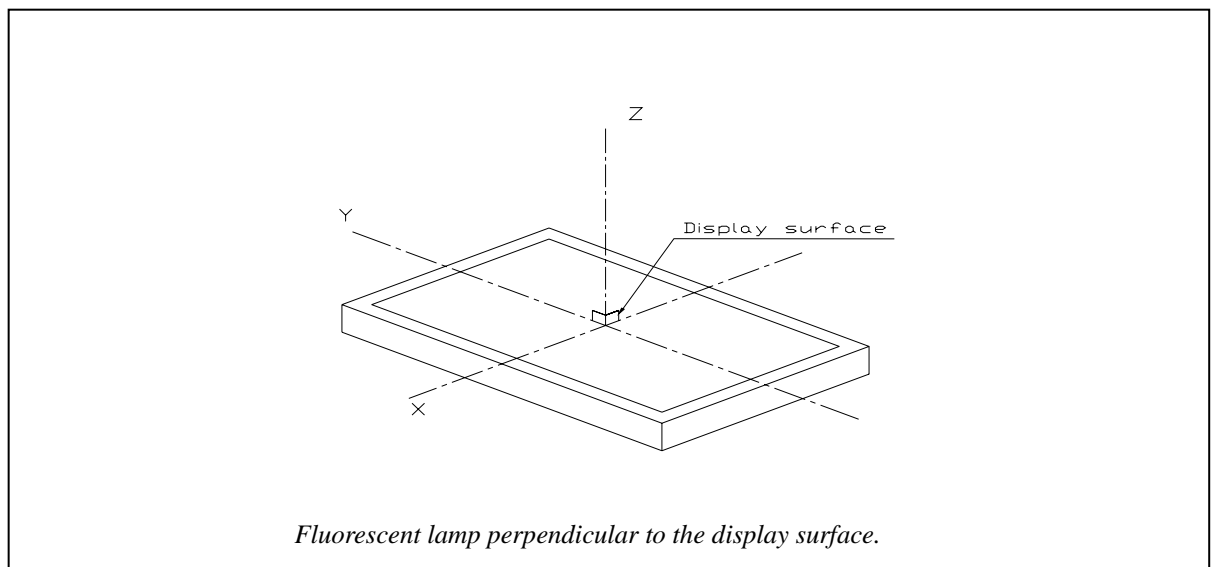
*Room temperature:  $20\pm 3^{\circ}\text{C}$*

*Humidity:  $65\pm 20\%RH$*

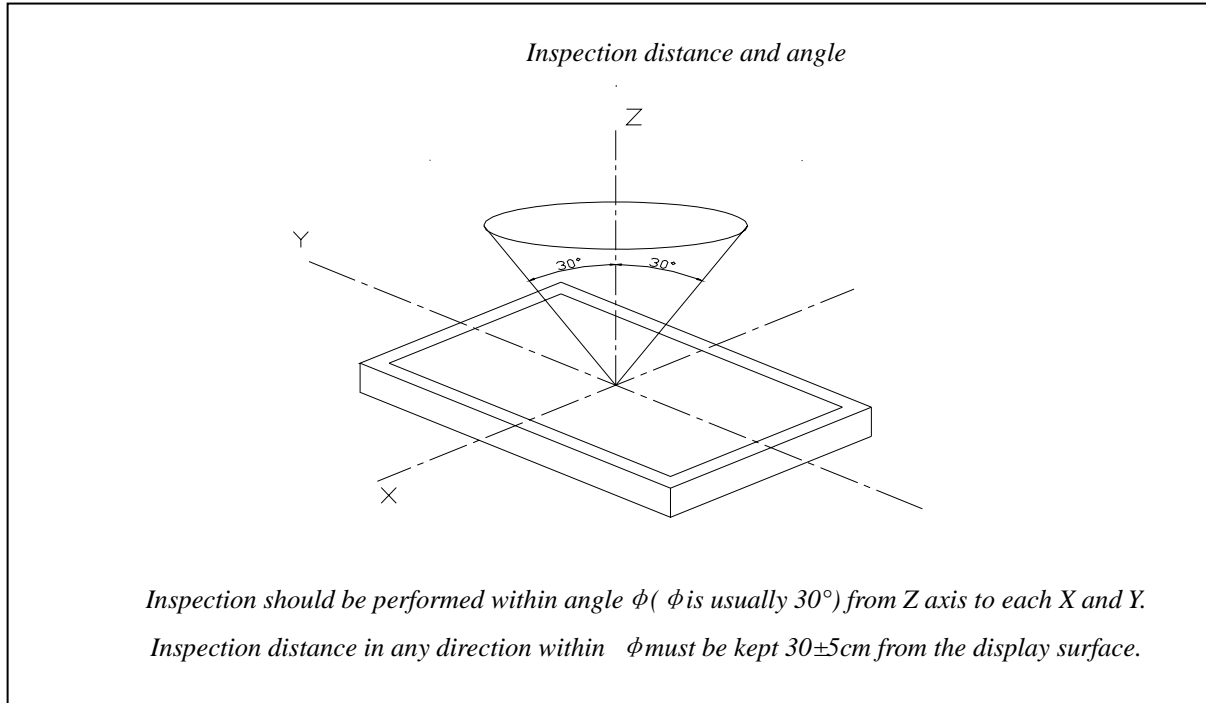
#### 8.1.2 The external visual inspection

*With a single 20-watt fluorescent lamp as the light source, the inspection was in the distance of 30cm or more from the LCD to the inspector's eyes .*

### 8.2 LIGHT METHOD



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## 8.3 Classification of defects

### 9.3.1 Major defect

*A major defect refers to a defect that may substantially degrade usability for product applications.*

### 9.3.2 Minor defect

*A minor defect refers to a defect which is not considered to be able substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation.*



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## 9. RELIABILITY

### 9.1 MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

### 9.2 TESTS

NO.	Test Item	Test condition	Criterion
1	High Temperature Storage	80°C±2°C 96H Restore 2H at 25°C Power off	After testing, cosmetic and electrical defects should not happen.
2	Low Temperature Storage	-30°C±2°C 96H Restore 2H at 25°C Power off	
3	High Temperature Operation	70°C±2°C 96H Restore 2H at 25°C Power on	
4	Low Temperature Operation	-20°C±2°C 96H Restore 4H at 25°C Power on	
5	High Temperature & Humidity Operation	60°C±2°C 90%RH 96H Power on	
6	Temperature Cycle	-30°C↔25°C↔80°C 30min 5min 30min after 10cycle, Restore 2H at 25°C Power off	
7	Vibration Test	10Hz~150Hz, 100m/s <sup>2</sup> , 120min	
8	Shock Test	Half-sinewave, 300m/s <sup>2</sup> , 11ms	1. After testing, cosmetic and electrical defects should not happen. 2. the product should remain at initial place 3. Product uncovered or package broken is not permitted.
9	Drop Test(package state)	800mm, concrete floor, 1corner, 3edges, 6 sides each time	